

Characterization of the Oxide-Semiconductor Interface in 4H-SiC/SiO₂ Structures using TEM and XPS

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Silicon carbide (SiC) is a very promising wide bandgap material for high power and high-temperature applications due to its native SiO₂ oxide, high thermal conductivity, and high bulk electron mobility [1]. Performance and reliability in these devices is limited however, by their low carrier mobility within the FET channel caused by electrically active defects at the oxide interface. A number of methods have been developed for improving the mobilities in fabricated devices, and the most prevalent of these is incorporation of nitrogen at the oxide interface through a post-oxidation nitric oxide (NO) anneal (POA) [2]. While the mechanisms behind the resulting device improvement and the interfacial structure are a matter of active research, the true nature of the interface is still not totally clear.

Distinct transition layers at the interface between SiC and SiO₂ have been previously observed by electron energy loss spectroscopy (TEM-EELS) and an inverse relationship was observed between the length of NO annealing time and the width of the transition region (w_{TL}) [3]. In order to gain a more thorough understanding of the chemical and electronic structure at this interface, devices in a variety of orientations and both with and without a POA have been investigated in this work using high resolution TEM (HRTEM), high-angle annular dark field imaging (HAADF-STEM), EELS, and angle resolved x-ray photoemission spectroscopy (AR-XPS). The aim of this study is to analyze how both device orientation (leading to atomic scale roughness) and post-oxidation processing affect various atomic scale properties, including the transition layers' composition and strain, as well as the electronic configuration and contributions from possible interfacial states.

HRTEM inspection and EELS measurements were made on a series of six samples, with varying orientations and processing. Oxide layers were grown on the epitaxial layer of 4H-SiC wafers with one of three orientations: Si-face (Si-terminated [0001] surface normal) on-axis, Si-face miscut by 4° (the orientation used in commercial applications), and a-face ([11 $\bar{2}$ 0] surface normal). For each of these orientations, one sample was analyzed prior to any NO POA process, and another that had received a 2hr POA. w_{TL} was measured by monitoring the edge onset energy of the Si-L_{2,3} EELS edge across the interface, as described in [3]. As shown in Figure 1a, the w_{TL} values on the Si-face were practically identical regardless of NO anneal, contradicting expectations. For all the Si-face samples, w_{TL} values were significantly lower than those measured previously on similar devices, indicating an overall improvement and that current mobility-limiting defects in state of the art devices may not be accurately probed through observation of the Si-L_{2,3} edge. The a-face devices did have slightly lower w_{TL} values, indicating that roughness (Figure 1b-g) at the interface may be a limiting factor in these devices.

To further probe the nature of the interfacial transition region, chemical depth profile experiments using AR-XPS have been performed. Using a spin-etch technique refined from previous work on the Si/SiO₂ interface [4], layers of oxide can be removed with sub-nm precision to carefully approach the SiC/SiO₂ interface with very little damage or adverse chemical modification (verified by identical XPS spectra

after etches on thicker oxide layers). This process was used to compare the near-interface region of oxides grown on Si-face 4H-SiC, both with and without an additional NO POA.

Detailed AR-XPS scans were performed on each element in question to investigate differences arising from the POA process and from changes in oxide thickness or interfacial strain. The Si-2*p* (Figure 1h) signal revealed three distinct states at the interface, corresponding to “bulk” SiO₂ and SiC, and an interfacial state. An additional state was present in samples that were fully etched, at an energy level slightly lower than the bulk oxide, but this was not observed in any samples that retained the original oxide, indicating that besides the interfacial states, all Si atoms in the oxide are fully complemented by O atoms. It is suspected that these lower energy states result from a monolayer of oxygen that cannot be removed by HF etching, though this state emerged at an energy level about 1eV higher than previous reports [7].

Examining the N-1*s* scans (Figure 1i), 4 distinct components were observed, and the N content was found to be localized entirely near the interface (not removed by the etching process) in a silicon nitride-like configuration. Furthermore, analysis of the C-1*s* components revealed significant C-O bonding at the interface, which appears to be reduced upon NO POA. [8]

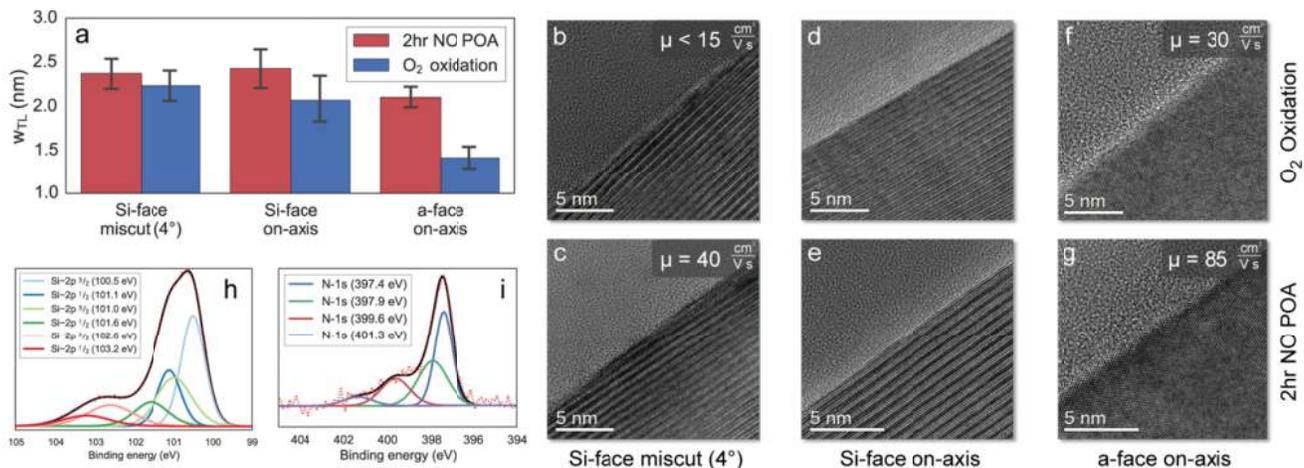


Figure 1: (a) Measurement of w_{TL} at the SiC/SiO₂ interface obtained by analysis of Si-*L*_{2,3} EELS line scans perpendicular to the interface (error bars represent 0.95 confidence intervals). (b-g) Representative HRTEM images of each interface. Conditions and orientation are indicated in the figure. Where known, representative peak field effect mobility (μ) values are given for similar samples [5-6]. (h) AR-XPS (scan was 70° relative to normal) results showing spin-orbit split components of the Si-2*p* orbital. (i) N-1*s* components present in an NO POA sample.

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